A Simulation Study on the Performance of Wafer Fabs with Hot Lots Under WIP Balance and Due Date Control Policies

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Abstract. In semiconductor wafer fabs, hot lots refer to a group of products which have high priority for various reasons, e.g, pilot products or due date commitments to customers. Hot lots are given the highest priority with the purpose of reducing their cycle time. However, hot lots often cause irregular WIP flow that has great impact on cycle time and throughput of regular lots. In this paper, we present a simulation study including two cases on handling degraded performance of regular lots under the control of minimum inventory variability scheduling (MIVS) and operation due date (ODD). In the first case, when hot lots represent 10% of total release, we propose to improve the pace of lot movement for MIVS and break dominance of due date control ODD. In the second case, as the percentage of hot lots increases to 30%, we apply a hierarchical dispatching scheme in which target cycle time is set higher for hot lots and regular lots. The simulation results show that for the first case, the compensatory methods are able to improve the performance of regular lots by overcoming deficiencies of MIVS and ODD; for the second case, it is important to establish a target cycle time if a trade-off is needed between hot lots and regular lots.

Introduction

Semiconductor wafer fabrication facilities (wafer fabs) contain hundreds of production equipment and dozens of kinds of wafer products. Each kind of product has a unique technologic process flow which includes hundreds of processing steps. There are many characteristics of wafer fabs, such as hot lots, re-entrant processing flows, batch tools, sequence dependent setups, unpredictable equipment failures and so on, which differentiate wafer fabs from other job shops and flow shops. In general, release rules and dispatching rules are two major ways that are applied to control the wafer fabs for the purpose of decreasing cycle time, cycle time variance and achieving on time delivery [1].

For traditional wafer fabs operating mass production, work-in-process (WIP) is the main concern in shop floor control since it has a major influence on overall manufacturing costs. To reduce the inventory level, WIP oriented dispatching rules are applied in these wafer fabs. For that purpose, minimum inventory variability scheduling (MIVS) [2] is the representative rule. MIVS considers both upstream and downstream operations. It gives the highest priority to an operation which has a high WIP and its downstream operation has a low WIP, in order to avoid starvation at downstream operations. In contrast, it gives the lowest priority to an operation which has a low WIP and its downstream operation has a high WIP. The MIVS intends to keep the WIP of each operation close to the average target WIP level. As many wafer fabs change from mass production to mass customization to satisfy customers, due dates become another critical factor. Due date oriented dispatching rules [3], e.g., earliest due date and operation due date (ODD) are applied to achieve on-time delivery in these wafer fabs. The ODD rule breaks up the slack time into as many segments as the number of operations of a lot, which means it considers due dates for all intermediate operations. The ODD value of operation i is defined as: $ODD = ReleaseTime + RPT(i) * DDFF$, where $RPT(i)$ denotes the raw processing time for a sequence of processing steps or operations from operation 1 to operation i (including operation i) and $DDFF$ denotes target due date flow factor which is the ratio of the target cycle time and the raw processing time of a lot.

Although different kinds of dispatching rules are already available for wafer fabs, shop floor control is no trivial task due to production variations, e.g., hot lots. Hot lots refer to a group of products that have the highest priority for various reasons, e.g., pilot products, process testing and due date commitments to customers. Hot lots are given high priority to reduce their cycle time. However, hot lots often cause an irregular WIP flow that has great impact on the cycle time and throughput of regular lots. A number of researchers have examined the impact of hot lots on the performance of wafer fabs. [4] considered hot lots as one of the production variabilities that affect overall cycle time and should be well managed. [5] carried out

ARGESIM Report 59 (ISBN 978-3-901608-93-3), p 381-388, DOI: 10.11128/arep.59.a59053

a simulation study to understand the impact of hot lots on the cycle time of regular lots. They demonstrated that as the ratio of hot lots increases, average cycle times and standard deviation of cycle times of regular lots increase drastically. [6] showed that hot lots cause production capacity loss, especially for the batch processing. [7] applied simulation to analyze the impact of different percentages of hot lots on the cycle time of two different products. To reduce the impact of hot lots on the overall cycle time of products, they developed rules-of-thumb to release appropriate amounts of hot lots to the wafer fabs. [8] developed an analytical method based on mean value analysis to predict the performance of wafer fabs in the presence of hot lots. The simulation results also demonstrate that hot lots have a significant impact on the mean cycle time, variance of cycle time and throughput rate of regular lots. [9] carried out a simulation study on the scheduling policies to minimize the cycle time of hot lots in batch processes.

In conclusion, hot lots have a significant impact on the performance of wafer fabs, in particular, the cycle time and throughput are degraded tremendously for regular lots. The researchers above focus on either small manufacturing lines or applying the first in first out (FIFO) dispatching policy. It is of much importance to examine hot lots in a complete wafer fabs with different shop floor dispatching policies like MIVS or ODD. Furthermore, as the ratio of hot lots increases, it is of practical interest to find a solution to improve the degraded performance of regular lots. We attempt to address these two issues in this study.

In this paper, we study two cases that are defined by the percentage of hot lots in wafer fabs. The first case, where wafer fabs contain 10% hot lots of the total release, is considered as low ratio of hot lots. Hot lots cause irregular WIP flow for regular lots since hot lots have priority at all stages of processing. Both MIVS and ODD rules can not successfully handle it. For MIVS, we focus on improving the pace of regular lots by introducing a flow factor (FF) rule. For ODD, we suggest to break the dominance of due date control to speed up lot movement. The second case, when the hot lots ratio is increased to 30%, the wafer fabs are running in an extreme manner. As the hot lots enter to the wafer fabs continuously, all resources are occupied by them. The consequence is that the regular lots can not be processed on time which causes serious congestion in front of tool groups. In this situation, we try to find a tradeoff between hot lots and regular lots to answer the question how the performance of the regular lots can be improved at the cost of performance of the hot lots.

This paper is organized as follows. In Section 1, we introduce the wafer fabs model used in this study. In Section 2, we present two study cases by describing the problem and solutions in detail. The conclusions can be found in Section 3.

1 Simulation Model

The whole wafer fabs dataset MIMAC6 from the Measurement and Improvement of MAnufacturing Capacities (MIMAC) project is used for this study. We refer the interested reader to [10] for details. The MIMAC6 is a typical complex wafer fabs model including:

- 9 products, 9 process flows, a maximum of 355 process steps. (Table 1 lists the basic information of the products)
- 24 wafers in a lot. 2777 lots are released per year under a fab loading of 100%.
- 104 tool groups (work-centers), 228 tools (machines). 46 single processing tool groups, 58 batching processing tool groups.
- Sequence dependent setups, rework, MTTR (mean time to repair), and MTBF (mean time between failures) of tool groups.

The simulation experiments are carried out by Factory eXplorer from WWK. The wafer fabs loading is set to 95%. The simulation length is 48 weeks with 3 replications, and the first 12 weeks are considered as warm-up periods.

Products	Raw Processing Time (days)	Time until next Release (hours)
B5C	17.6	30.4
B6HF	16.6	92.9
C4PH	10.9	43.9
C5F	15.1	36.4
C5P	11.8	10.9
C5PA	13.5	17.2
C6N3	14.9	47.6
C6N2	13.2	41.1
OX2	12.8	35.2

Table 1: Basic information of products in MIMAC6 model.

2 Simulation Cases

2.1 Low Ratio of Hot Lots

Before we introduce hot lots into the MIMAC6 wafer fabs, the MIVS and ODD rules are utilized for shop floor control, respectively. They are represented as 'MIVS(1)' in Table 2 and 'ODD(1)' in Table 3. For the first study case, according to Table 1 product 'B5C' comprises approximately 10% of total release. Thus, product 'B5C' is considered as hot lot, and other products are considered as regular lots. Thus, the dispatching policies are changed to hierarchical priorities which are shown as 'MIVS(2)' in Table 2 and 'ODD(2)' in Table 3. The hot lots have priority 1, and if two hot lots have the same priority, FIFO is used for tie-breaking. The regular lots have priority 2, and if two regular lots have the same priority, the MIVS and ODD rules are used for tie-breaking, respectively.

When the hot lots obtain higher priority over the regular lots at all stages of processing, a large number of regular lots pile up in front of tool groups. The fact is that the shortcomings of MIVS and ODD rules are magnified to certain extent.

Problem and Solution for MIVS.

The MIVS rule focuses on balancing WIP to reduce average cycle time. Nevertheless, it ignores the importance of good pace of lot movement. It would rather push a lot with less queue time to balance downstream tool-groups than push a lot with a long queue time, which leads to a degraded performance of cycle time variance. In a tool-group, after processing hot lots the MIVS rule faces a huge challenge as a large number of regular lots wait in queue. In order to overcome the drawback, the flow factor (FF) rule is applied to improve the WIP flow of regular lots.

The FF rule is an extension from a performance indicator called flow factor. It is a dynamic dispatching rule based on the ratio between accumulated cycle time and accumulate raw processing time [11], *FF = AccumulatedCycleTime / AccumulatedRawProcessingTime*. Obviously, a small flow factor is desirable as it indicates a low cycle time. The FF rule is expected to improve the pace of lot movement as it attempts to keep lots going through the wafer fabs with the same flow factor. The FF rule is incorporated into the hierarchical dispatching to better distinguish lots that obtain the same priority from the MIVS rule, which is depicted as 'MIVS(3)' in Table 2. When two lots obtain the same priority from MIVS, the one with a higher FF value is preferred.

Hierarchical dispatching policies based on MIVS (10% ratio of hot lots)		
MIVS(1)	**MIVS(2): Hot lots + MIVS**	**MIVS(3): Hot lots + (MIVS + FF)**
All lots: -> MIVS	**Priority 1**: Hot lots: -> FIFO **Priority 2**: Regular lots: -> MIVS	**Priority 1**: Hot lots: -> FIFO **Priority 2**: Regular lots: -> MIVS -> FF

Table 2: Three hierarchical dispatching policies based on MIVS.

Problem and Solution for ODD.

In contrast to the MIVS rule, even though the hot lots disturb the WIP flow of the regular lots, the ODD rule still manages the difficulty to achieve good pace of movement, which brings an excellent performance of cycle time variance. The fact is although regular lots have loose target due dates, some of them are already close to their due dates or even late after hot lots finish processing. The ODD rule overemphasizes the pace of movement. Thus, the fresh regular lots have to wait for the late regurlar lots. This procedure leads to slow movement. As a result, the ODD rule produces high cycle time for regular lots. We realize that breaking the dominance of ODD rule is the way to accomplish fast movement for regular lots.

The modified operation due date rule (MOD) is applied in this case. The MOD rule is a combination of ODD and shortest processing time (SPT). It is expressed as follows: *MOD = Max(ODD, now+PT)*, where *ODD* is the operation due date of a lot, now is current time and *PT* is the processing time of a lot. A smaller MOD value indicates a higher priority. The MOD rule has the potential to solve the problem of ODD because it performs like the SPT rule when the due date becomes tight, and the SPT rule aims at achieving low cycle times. The dispatching policy with the MOD rule is listed as 'ODD(3)' in Table 3.

Hierarchical dispatching policies based on ODD (10% ratio of hot lots)		
ODD(1)	**ODD(2): Hot lots + ODD**	**ODD(3): Hot lots + (ODD + SPT)**
All lots: -> ODD	**Priority 1**: Hot lots: -> FIFO **Priority 2**: Regular lots: -> ODD	**Priority 1**: Hot lots: -> FIFO **Priority 2**: Regular lots: -> ODD+SPT

Table 3: Three hierarchical dispatching policies based on ODD.

Simulation Results.

The simulation results are presented in Tables 4 and 5. Cycle time, cycle time variance, cycle time upper percentile 95% and throughput are considered as performance measure.

Table 4 shows results from the dispatching policies in Table 2. The 'MIVS(1)' policy produces the results without hot lots in the wafer fabs. For the 'MIVS(2)', when product 'B5C' is introduced as hot lot, the performance of regular products is degraded. However, the overall performance of the wafer fabs is similar to the case of 'MIVS(1)'. The problem is that the 'MIVS(2)' policy produces particularly high cycle time variance and cycle time upper percentile 95% for products 'C4PH' and 'C6N2'. The 'MIVS(3)' policy utilizing the FF rule successfully solves the problem and outperforms 'MIVS(2)' for all performance measures. After processing hot lots in tool groups, it is crucial that the combination of MIVS and FF selects the lot with high cycle time (high flow factor) to balance WIP. On one hand it has ability to lower cycle time, on the other hand it manages to improve cycle time variance. In addition, the 'MIVS(3)' is able to increase throughput compared to the 'MIVS(2)'.

Similarly, Table 5 demonstrates the results from the dispatching policies in Table 3. After the introduction of hot lots, 'ODD(2)' is still able to achieve good performance of cycle time variance. Whereas, the cycle time performance of regular products is significantly affected. In this case, it is necessary to break the dominance of due date control. By introducing the SPT rule, the 'ODD(3)' policy manages to reduce the cycle time of regular products, although the cycle time variance is slightly degraded. It achieves better thoughput performance as well.

	Avg. Cycle Time (days)			Cycle Time Variance (days^2)			Cycle Time Upper Pct. 95% (days)			Throughput (lots)		
Products	**MIVS(1)**	**MIVS(2)**	**MIVS(3)**	**MIVS(1)**	**MIVS(2)**	**MIVS(3)**	**MIVS(1)**	**MIVS(2)**	**MIVS(3)**	**MIVS(1)**	**MIVS(2)**	**MIVS(3)**
B5C	31.3	22.6	22.5	2.5	0.4	0.2	34.7	24.0	23.7	227	234	236
B6HF	30.1	32.1	30.3	1.7	1.7	1.5	34.7	35.3	32.0	73	74	74
C4PH	24.7	25.6	23.2	2.9	4.5	1.8	28.3	29.9	27.3	159	161	162
C5F	29.1	29.9	30.6	2.5	2.1	1.0	33.3	34.0	33.3	191	191	191
C5P	23.9	25.5	23.9	1.6	1.2	0.7	27.3	27.7	26.0	649	645	647
C5PA	26.0	26.6	26.6	1.8	1.4	1.4	29.3	29.7	29.3	408	406	409
C6N3	29.3	29.9	28.8	1.8	1.4	0.9	32.7	34.0	31.0	148	145	147
C6N2	26.5	28.3	25.9	1.6	3.2	1.6	30.0	31.8	28.0	172	172	172
OX2	25.8	27.0	25.7	2.4	1.6	1.0	29.7	30.7	28.0	200	199	200
Summary	27.4	27.5	26.3				32.7	32.0	30.8	2227	2227	2238

The wafer fabs loading is 95%;
B5C: Hot lot; MIVS(1): There are no hot lots in wafer fabs; MIVS(2): Hot lots + MIVS; MIVS(3): Hot lots + (MIVS + FF).

Table 4: Four performance measure comparison among MIVS(1), MIVS(2) and MIVS(3).

	Avg. Cycle Time (days)			Cycle Time Variance (days^2)			Cycle Time Upper Pct. 95% (days)			Throughput (lots)		
Products	ODD(1)	ODD(2)	ODD(3)	ODD(1)	ODD(2)	ODD(3)	ODD(1)	ODD(2)	ODD(3)	ODD(1)	ODD(2)	ODD(3)
B5C	35.9	22.5	22.5	0.3	0.4	0.3	37.3	24.0	23.7	224	234	234
B6HF	34.2	36.2	31.3	0.9	0.7	2.3	36.0	37.3	36.0	74	74	74
C4PH	21.6	23.6	24.5	0.3	0.4	1.9	23.0	24.0	23.3	163	163	162
C5F	32.0	33.9	31.5	0.5	0.6	2.0	33.3	34.7	34.3	190	189	192
C5P	24.0	25.8	23.8	0.2	0.4	0.7	25.3	26.3	25.3	650	648	648
C5PA	26.7	28.7	27.7	0.5	0.4	1.1	28.0	29.7	30.3	408	406	409
C6N3	28.8	29.8	29.9	0.9	1.0	1.9	30.7	32.0	31.0	147	146	146
C6N2	25.1	27.3	26.9	0.8	0.6	1.6	27.0	28.6	28.7	173	171	172
OX2	25.3	27.3	25.5	0.2	0.6	1.6	26.3	28.7	27.3	200	200	200
Summary	28.1	28.3	27.0				36.7	37.7	32.7	2229	2231	2237
The wafer fabs loading is 95%; B5C: Hot lot; ODD(1): There are no hot lots in wafer fabs; ODD(2): Hot lots + ODD; ODD(3): Hot lots + (ODD + SPT); Target due date flow factor for regular products: 2.5.												

Table 5: Four performance measure comparison among ODD(1), ODD(2) and ODD(3).

2.2 High Ratio of Hot Lots

Product 'C5P' represents approximately 30% of the total release. The second case is to study the performance of the wafer fabs when 'C5P' is considered as hot lot. As a great many hot lots are processed everywhere, the wafer fabs are operated in an extreme manner. All resources including tools and operators are occupied by the hot lots. In addition, the hot lots enter to the wafer fabs continually. As a result, some regular lots have no chance to go through the wafer fabs, which causes serious congestion in front of tool groups. The wafer fabs are running at an extremely high WIP level.

We notice that some low volume products which share critical tool groups with the hot lots are affected the most. In the MIMAC6 wafer fabs, 'C4PH' and 'OX2' are two low volume products which have the most degraded performance. Even 'MIVS(3)' and 'ODD(3)', which were capable of improving performance for regular lots in the first case, can not sufficiently handle this issue. Since the amount of hot lots is huge, on one hand, the only way to break their monopoly is to introduce high priority for competing lots; On the other hand, the performance of hot lots is still the major concern. Thus, firstly the affected low volume products are defined as 'urgent lots' which are assigned priority 2, and the other regular lots have priority 3. Furthermore, the class of priority 1 is divided into 3 sub-levels by means of target cycle time comparison.

- Sub-priority 1 is assigned to the hot lots which are late for their target cycle time of the current step. The target cycle time for each step is defined as follows: *TargetCT = ReleaseTime + PRT(i)*FF*, where *RPT(i)* denotes the raw processing time for a sequence of processing steps or operations from operation 1 to operation *i* (including operation *i*) and *FF* denotes the target flow factor.
- Some lots from urgent lots class obtain sub-priority 2 if they are late for their target cycle time.
- If the hot lots are on schedule compared to their target cycle times, they are assigned sub-priority 3. The hierarchical dispatching policies are represented as 'MIVS(4)' and 'ODD(4)' in Table 6.

Sub-priority 1 ensures that the late hot lots receive needed resources to catch up with their target cycle time. The purpose of sub-priority 2 is to make a trade-off between hot lots and urgent lots. In fact, whether the performance of urgent lots can be improved depends on the amount of hot lots with sub-priority 1. In other words, if the target cycle times are tight, most of the hot lots are late, then the urgent lots have to wait till the hot lots finish processing. On the contrary, if the target cycle times are loose, the urgent lots are able to compete with the hot lots for resources since some hot lots have sub-priority 3. In the following experiment, the target cycle times of hot lots are defined from tight to loose. We intend to find out if the performance of urgent lots can be improved at the

cost of good performance of the hot lots.

Hierarchical dispatching policies based on MIVS and ODD (30% ratio of hot lots)	
MIVS(4): Hot lots + Urgent lots + (MIVS + FF)	**ODD(4):** Hot lots + Urgent lots + (ODD + SPT)
Priority 1: **Priority 1.1**: Hot lots: -> Accu.CT>=TargetCT -> FIFO **Priority 1.2**: Urgent lots: -> Accu.CT>=TargetCT -> FIFO **Priority 1.3:** Hot lots: -> Accu.CT<TargetCT -> FIFO **Priority 2**: Urgent lots: -> MIVS -> FF **Priority 3**: Regular lots: -> MIVS -> FF	**Priority 1**: **Priority 1.1**: Hot lots: -> Accu.CT>=TargetCT -> FIFO **Priority 1.2**: Urgent lots: -> Accu.CT>=TargetCT -> FIFO **Priority 1.3**: Hot lots: -> Accu.CT<TargetCT -> FIFO **Priority 2**: Urgent lots: -> ODD+SPT **Priority 3**: Regular lots: -> ODD+SPT
Accu.CT is accumulated cycle time for step, TargetCT is target cycle time for step.	

Table 6: Hierarchical dispatching policies by introduction of urgent lots and target cycle time.

Simulation Results.

At first we examine the simulation results in Table 7. The 'MIVS(3)' policy, which achieves good performance with the 10% ratio of hot lots, shows opposite behavior with a 30% ratio of hot lots. We focus on products 'C4PH' and 'OX2' which are affected the most by hot lots. A large number of lots from 'C4PH' and 'OX2' are not able to go through the wafer fabs. Thus, 'MIVS(3)' produces tremendous cycle times and low throughput for them. We notice that 'C4PH' and 'OX2' are not able to be processed unless they obtain high priority to complete with the hot lots. 'MIVS(4)' is developed for this purpose. According to the average cycle time and cycle time upper percentile 95% of 'C5P' (hot lot), its actual cycle time flow factors are calculated between 1.4 to 1.6. To make sure the hot lots provide their priorities to the urgent lots, the target cycle time flow factors of 'C5P' are set from 1.5 (tight) to 1.9 (loose) with an increment of 0.2. The target cycle time flow factor of 'C4PH' and 'OX2' is set 2.0. We expect more and more urgent lots can finish processing as the target cycle time flow factors of 'C5P' change from 1.5 to 1.9.

Apparently, the throughput performance is improved. The 'MIVS(4)FF:1.9' manages to finish 112 lots for 'C4PH' and 143 lots for 'OX2', which is significantly improved compared to 'MIVS(3)'. 'C4PH' and 'OX2' struggle to obtain high priority. However, due to a large amount of hot lots, as long as the hot lots meet their target cycle times, 'C4PH' and 'OX2' lose chances to be processed. As a consequence, the cycle time and variance performance can not be improved greatly. In Table 8, 'ODD(4)' policy shows a similar behavior as 'MIVS(4)'.

	Avg. Cycle Time (days)				Cycle Time Variance (days^2)				Cycle Time Upper Pct. 95% (days)				Throughput (lots)			
Products	MIVS(3)	MIVS(4) FF:1.5	MIVS(4) FF:1.7	MIVS(4) FF:1.9	MIVS(3)	MIVS(4) FF:1.5	MIVS(4) FF:1.7	MIVS(4) FF:1.9	MIVS(3)	MIVS(4) FF:1.5	MIVS(4) FF:1.7	MIVS(4) FF:1.9	MIVS(3)	MIVS(4) FF:1.5	MIVS(4) FF:1.7	MIVS(4) FF:1.9
B5C	31.8	35.4	35.8	36.4	2.7	1.1	1.5	1.2	36.0	38.7	38.7	38.7	229	225	225	224
B6HF	31.0	34.1	34.5	34.1	2.8	1.0	0.8	1.3	36.0	37.3	37.3	38.0	76	75	74	74
C4PH	83.5	78.0	77.3	72.1	5.4	6.4	5.1	6.5	178.7	154.7	138.7	126.7	74	92	105	112
C5F	29.5	31.1	31.5	32.0	2.6	1.3	1.8	1.3	33.3	34.7	34.0	34.7	192	192	190	190
C5P	16.6	16.9	16.9	17.1	0.5	0.4	0.5	0.6	18.3	18.3	18.3	18.7	668	666	666	664
C5PA	26.1	26.4	26.6	27.2	2.2	1.3	1.4	1.3	29.3	29.3	29.3	30.0	407	410	409	405
C6N3	29.8	28.9	29.2	29.8	2.7	1.5	1.3	1.3	34.0	32.3	32.0	32.7	147	148	146	146
C6N2	26.9	25.4	25.6	26.1	2.7	1.0	1.2	1.2	31.0	28.3	28.3	28.7	173	173	172	172
OX2	73.9	73.5	72.3	70.6	6.0	5.0	4.0	6.6	133.3	144.0	133.3	124.0	93	116	129	143
Summary	38.8	38.8	38.8	38.4					58.7	53.3	82.7	84.0	2059	2097	2116	2130

The wafer fabs loading is 95%;
C5P: Hot lot; C4PH and OX2: Urgent lots;
MIVS(3): There are hot lots and regular lots (no urgent lots) in wafer fabs, Hot lots + (MIVS + FF);
MIVS(4): Introduction of urgent lots, Hot lots + Urgent lots + (MIVS + FF);
FF: Target cycle time flow factor.

Table 7: Four performance measure comparison among MIVS(3), MIVS(4)FF:1.5, MIVS(4)FF:1.7 and MIVS(4)FF:1.9.

	Avg. Cycle Time (days)				Cycle Time Variance (days^2)				Cycle Time Upper Pct. 95% (days)				Throughput (lots)			
Products	MIVS(3)	MIVS(4) FF:1.5	MIVS(4) FF:1.7	MIVS(4) FF:1.9	MIVS(3)	MIVS(4) FF:1.5	MIVS(4) FF:1.7	MIVS(4) FF:1.9	MIVS(3)	MIVS(4) FF:1.5	MIVS(4) FF:1.7	MIVS(4) FF:1.9	MIVS(3)	MIVS(4) FF:1.5	MIVS(4) FF:1.7	MIVS(4) FF:1.9
B5C	33.9	35.3	35.3	35.9	0.8	0.9	1.0	1.2	36.7	38.0	38.7	40.0	225	226	226	225
B6HF	32.0	33.7	33.6	34.1	1.8	0.9	1.5	2.0	35.3	36.7	36.7	38.0	75	75	74	75
C4PH	120.0	90.8	73.6	76.8	4.2	5.2	6.2	5.4	197.3	152.0	152.0	114.7	60	84	94	92
C5F	29.8	31.2	31.0	31.6	1.0	1.3	1.0	1.6	32.7	34.0	34.7	36.0	192	191	191	191
C5P	17.1	17.0	17.0	17.2	0.8	0.4	0.4	0.5	19.7	19.9	20.1	20.9	664	666	666	666
C5PA	25.0	26.2	26.2	26.8	0.9	1.1	1.0	1.3	27.7	28.7	29.3	30.7	409	410	409	409
C6N3	27.2	28.4	28.3	28.9	1.3	1.3	1.6	1.7	30.3	30.7	31.3	32.7	148	147	148	148
C6N2	23.7	24.9	24.8	25.4	0.9	0.9	0.9	1.0	26.3	27.0	27.7	29.0	173	173	172	173
OX2	122.7	91.8	68.7	75.7	5.1	10.9	13.9	6.0	208.0	146.7	154.7	138.7	83	116	118	122
Summary	47.9	42.1	37.6	39.1					72.0	77.3	93.3	96.0	2029	2088	2098	2101

The wafer fabs loading is 95%;
C5P: Hot lot; C4PH and OX2: Urgent lots;
ODD(3): There are hot lots and regular lots (no urgent lots) in wafer fabs, Hot lots + (ODD + SPT);
ODD(4): Introduction of urgent lots, Hot lots + Urgent lots + (ODD + SPT);
FF: Target cycle time flow factor; Target due date flow factor for regular products: 2.5.

Table 8: Four performance measure comparison among ODD(3), ODD(4)FF:1.5, ODD(4)FF:1.7 and ODD(4)FF:1.9.

3 Conclusions

In this paper, we present a simulation study on handling the degraded performance of regular lots caused by hot lots. Even though the wafer fabs are operated by well-known WIP balance and due date control policies, i.e., MIVS and ODD, the hot lots still have great impact on cycle time and throughput of the regular lots. Thus, we present two cases to discuss the problem of different ratios of hot lots and intend to find out corresponding solutions.

The first case, when the hot lots comprise 10% of total release, is considered as low ratio case. In order to overcome the deficiencies of the MIVS and ODD rules, we propose to apply a flow factor rule to improve the pace of movement for the MIVS rule, and a shortest processing time rule to break the dominance of due date control for the ODD rule. The simulation results indicate that the proposed methods are able to improve the performance of regular lots.

As the percentage of hot lots are increased to 30%, the second case is considered as high ratio case of hot lots. Because the hot lots occupy resources everywhere in the wafer fabs, the performance of the regular lots degrades severely. In particular, some low volume products which share critical resources with the hot lots are affected the most. Under this circumstance, the methods proposed in the first case are not able to tackle the problem. Therefore, we propose a hierarchical dispatching scheme in which 1) high priorities are assigned to the most affected products; 2) target cycle times are established for the hot lots and the most affected products. The simulation results tell us that when the wafer fabs are running with large amount of hot lots, a trade-off between hot lots and the most affected products is necessary. It is important to set up target cycle times so that we can determine if the improvement of the most afftected products is achieved at the cost of a good performance of the hot lots.

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